**2/4 B.Tech. FIRST SEMESTER**
**COMPUTER ORGANISATION**

**CS3T4** **Required** **Credits: 4**

**Lecture: 4 periods/week** **Internal assessment: 30 marks**
**Tutorial: 1 period /week** **Semester end examination: 70 mark**

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**Course context and Overview:** Introduction to computer organization. Computer instruction set. Machine language. Data processing. Arithmetic unit: Carry look-ahead adders, Subtractors, and shifters. Logic unit. Combinational and sequential multipliers and dividers. Floating-point number representation and arithmetic. Data path design. Control unit design. Microprogramming. Pipelining. Memory Hierarchy.

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**Prerequisites: Digital Logic Design and Basic Electronics**

**Objectives:**

1. To have a thorough understanding of the basic structure and operation of a digital computer.
2. To discuss in detail the operation of the arithmetic unit including the algorithms & implementation of fixed-point and floating-point addition, subtraction, multiplication & division.
3. To study the hierarchical memory system including cache memories and virtual memory.
4. To study the different ways of communicating with I/O devices and standard I/O interfaces.
5. To study the concept of pipelining and the way it can speed up the processing, Instruction pipelining and RISC pipelining.
6. To study the basic characteristics of Multiprocessors and Interconnection structures and interprocessor communication.

**Learning outcomes**:

Ability to:

1. Understand the notations in register transfer language, memory and micro-operations used in computer.
2. Design basic building blocks of a computer like ALU, registers, processor and memory at gate level.
3. Analyze the organization of various memory types and I/O devices.
4. Develop arithmetic operations for digital computer system.
5. Distinguish the performance of pipelining and non pipelining environment in a processor.
6. Understand the multi processor concepts.

**UNIT-I**

**REGISTER TRANSFER AND MICRO-OPERATIONS:**

Register Transfer Language, Register Transfer, Bus and memory Transfers, Arithmetic Micro-operations, Logic Micro-operations, Shift Micro-operations, Arithmetic Logic Shift

Unit.

**UNIT-II**
**BASIC COMPUTER ORGANIZATION AND DESIGN:**
Instruction codes, Computer Registers, Computer Instructions, Timing and Control, Instruction cycle, Memory-Reference Instructions, Input-Output and Interrupt, Design of Basic Computer.

**UNIT-III**
**MICRO PROGRAMMED CONTROL:**
Control Memory, Address Sequencing, Micro-Program example, Design of Control Unit.

CENTRAL PROCESSING UNIT: General register Organization, Stack Organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation, Program Control, Reduced Instruction Set Computer (RISC).

**UNIT-IV**
**COMPUTER ARITHMETIC:**
Addition and Subtraction, Multiplication Algorithms, Division Algorithms, Floating-point Arithmetic operations.

**UNIT-V**
**MEMORY ORGANIZATION:**
Memory Hierarchy, Main Memory, Auxiliary memory, Associative Memory, Cache Memory, Virtual Memory, Memory Management hardware.

**UNIT-VI**
**INPUT-OUTPUT ORGANIZATION:**
Peripheral Devices, Input-output Interface, Asynchronous Data Transfer, Modes of Transfer, Priority Interrupt, Direct Memory Access (DMA),Input-Output Processor, Serial Communication.

**UNIT-VII**
**PIPELINING AND VECTOR PROCESSING:**
Parallel processing, Pipelining, Arithmetic pipeline, Instruction pipeline, Risc pipeline.

**UNIT-VIII**
**MULTIPROCESSORS:**
Characteristics of multiprocessors, Interconnection structures, Inter processor arbitration, Interprocessor communication and synchronization.

## Learning Resources

**TEXTBOOK:**

1. 'Computer System Architecture', Morris M. Mano, 3rd edition,pearson/Prentice Hall India.

**REFERENCE BOOKS:**

1. Computer Organization and Architecture, William Stallings ,8th edition,PHI

2. Computer Organization, Carl Hamachar, Vranesic, McGraw Hill.